

# Curriculum Vitae

## Personal Data

Daniel Ángel Jiménez  
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**Citizenship** United States of America

## Education

- 2002 Ph.D. Computer Sciences, The University of Texas at Austin  
Thesis title: *Delay-Sensitive Branch Predictors for Future Technologies*
- 1994 M.S. Computer Science, The University of Texas at San Antonio  
Thesis title: *Methods for Satisfying Hard Boolean Formulas*
- 1992 B.S. Computer Science and Systems Design, The University of Texas at San Antonio

## Research Interests

Computer architecture; characterizing and exploiting the predictability of programs.

Compilers; low-level code-improving transformations such as code-reordering for improving instruction fetch bandwidth.

## Employment History

- 2007–present Associate Professor. Department of Computer Science, The University of Texas at San Antonio.
- 2008–present Associate Professor. Department of Computer Science, Rutgers University (*currently on leave*).
- 2002–2008 Assistant Professor. Department of Computer Science, Rutgers University.
- 2005 Visiting Research Faculty. Department of Computer Architecture, Technical University of Catalonia (UPC), Barcelona, Spain.
- 1999–2001 Research Assistant. Department of Computer Sciences, The University of Texas at Austin, under Prof. Calvin Lin.
- 1996–1999 Instructor/Research. Department of Rehabilitation Medicine, The University of Texas Health Science Center at San Antonio.
- 1996–1998 Instructor. Division of Computer Science, The University of Texas at San Antonio.
- 1995,1999 Teaching Assistant. Department of Computer Sciences, The University of Texas at Austin.
- 1994–1995 Programmer/Analyst. Department of Rehabilitation Medicine, The University of Texas Health Science Center at San Antonio.
- 1992–1994 Teaching Assistant. Division of Mathematics, Computer Science, and Statistics, The University of Texas at San Antonio.

## Journal Articles

Chunling Hu, Daniel A. Jiménez, Ulrich Kremer, *Combining Edge Vector and Event Counter for Time-dependent Power Behavior Characterization*, Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC) Vol. 2, No. 1, pp. 82–101, 2007.

Gabriel Loh and Daniel A. Jiménez, *Modulo Path History for the Reduction of Pipeline Overheads in Path-Based Neural Branch Predictors*, International Journal of Parallel Programming (IJPP), Published January 2008.

Daniel A. Jiménez, *Generalizing Neural Branch Prediction*, submitted August 2006 to ACM Transactions on Architecture and Code Optimization (*accepted as of May 2007*).

Chunling Hu, Daniel A. Jiménez, Ulrich Kremer, *An Evaluation Infrastructure for Power and Energy Optimizations*, International Journal of Embedded Systems (IJES) Vol. 3, No. 1/2, pp 31–42, 2007.

Daniel A. Jiménez, *Improved Latency and Accuracy for Neural Branch Prediction*, ACM Transactions on Computer Systems (TOCS), Vol. 23, No. 2, pp. 197–218, May 2005.

Daniel A. Jiménez, *Idealized Piecewise Linear Branch Prediction*, The Journal of Instruction-Level Parallelism (JILP), Vol. 7, April 2005.

Daniel A. Jiménez and Calvin Lin, *Neural Methods for Dynamic Branch Prediction*, ACM Transactions on Computer Systems (TOCS), Vol. 20, No. 4, pp. 369–397, November 2002.

## Refereed Conference Papers

Renée St. Amant, Daniel A. Jiménez, and Doug Burger, *Low-Power, High-Performance Analog Neural Branch Prediction*, Proceedings of the 41st International Symposium on Microarchitecture (MICRO-41), Lake Como, Italy, November 2008 (to appear). Acceptance rate: 19%.

Miquel Pericàs, Adrian Cristal, Ruben González, Daniel A. Jiménez, Alex Weidenbaum, and Mateo Valero, *A Two-Level Load/Store Queue Based on Execution Locality*, Proceedings of the International Symposium on Computer Architecture (ISCA), Beijing, China, June 2008. Acceptance rate: 14%.

Miquel Pericàs, Adrian Cristal, Ruben González, Daniel A. Jiménez, and Mateo Valero, *A Flexible Heterogeneous Multi-Core Architecture*, Proceedings of the International Conference on Parallel Architectures and Compilation Technologies (PACT), Braslov, Romania, September 2007. Acceptance rate: 19%.

Chunling Hu, Daniel A. Jiménez and Ulrich Kremer, *Efficient Program Power Behavior Characterization*, Proceedings of the 2007 International Conference on High Performance Embedded Architectures & Compilers (HiPEAC-2007), January 2007. Acceptance rate: 29%.

Daniel A. Jiménez and Gabriel H. Loh, *Controlling the Power and Area of Neural Branch Predictors for Practical Implementation in High-Performance Processors*, Proceedings of the 18th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2006), October, 2006. Acceptance rate: 31%.

Miquel Pericàs, Adrian Cristal, Ruben González, Daniel A. Jiménez, and Mateo Valero, *A Decoupled Kilo-Instruction Processor*, Proceedings of the 12th International Symposium on High Performance Computer Architecture (HPCA-12), pp. 52-63, February, 2006. Acceptance rate: 15%.

Miquel Pericàs, Ruben González, Adrian Cristal, Daniel A. Jiménez, and Mateo Valero, *Chained In-Order/Out-of-Order DoubleCore Architecture*, Proceedings of the 17th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), pp 55-62, October 2005. Acceptance rate: 35%.

Miquel Pericàs, Adrian Cristal, Ruben González, Daniel A. Jiménez, and Mateo Valero, *Exploiting Execution Locality with a Decoupled Kilo-Instruction Processor*, Proceedings of the 6th International Symposium on High Performance Computing (ISHPC-VI), September 2005.

Daniel A. Jiménez, *Piecewise Linear Branch Prediction*, Proceedings of the 32nd International Symposium on Computer Architecture (ISCA-32), pp. 382-393, June 2005. Acceptance rate: 23%.

Daniel A. Jiménez, *Code Placement for Improving Dynamic Branch Prediction Accuracy*, Proceedings of the ACM SIGPLAN 2005 Conference on Programming Language Design and Implementation (PLDI), pp. 107–116, June, 2005. Acceptance rate: 21%.

Daniel A. Jiménez, *Fast Path-Based Neural Branch Prediction*, Proceedings of the 36th Annual International Symposium on Microarchitecture (MICRO-36), pp. 243–252, San Diego, CA, December 3-5, 2003. Acceptance rate: 26%.

Daniel A. Jiménez, *Reconsidering Complex Branch Predictors*, Proceedings of the Ninth International Symposium on High Performance Computer Architecture (HPCA-9), pp. 43–52, Anaheim, CA, February 2003. Acceptance rate: 22%.

Daniel A. Jiménez, Heather L. Hanson and Calvin Lin, *Boolean Formula-Based Branch Prediction for Future Technologies*, Proceedings of the International Conference on Parallel Architectures and Compilation Technologies (PACT), pp. 97–106, Barcelona, Spain 2001. Acceptance rate: 21%.

Daniel A. Jiménez and Calvin Lin, *Perceptron Learning for Predicting the Behavior of Conditional Branches* (poster), Proceedings of the 2001 INNS-IEEE International Joint Conference on Neural Networks (IJCNN), pp. 2122–2126, Washington, DC, 2001.

Daniel A. Jiménez and Calvin Lin, *Dynamic Branch Prediction with Perceptrons*, Proceedings of the 7th International Symposium on High Performance Computer Architecture (HPCA-7), pp. 197–206, Monterrey, Mexico, January 20-24, 2001. Acceptance rate: 24%.

Daniel A. Jiménez, Stephen W. Keckler and Calvin Lin, *The Impact of Delay on the Design of Branch Predictors*, Proceedings of the 33rd Annual International Symposium on Microarchitecture (MICRO-33), pp. 67–76, Monterey, California, December 10-13, 2000. Acceptance rate: 31%.

Daniel A. Jiménez and Nicolas Walsh, *Dynamically Weighted Ensemble Neural Networks for Classification*, Proceedings of the 1998 INNS-IEEE International Joint Conference on Neural Networks (IJCNN), pp. 753-756, Anchorage, Alaska 1998.

Daniel A. Jiménez, Tom Darm, Bill Rogers and Nicolas Walsh, *Locating Anatomical Landmarks for Prosthetics Design Using Ensemble Neural Networks*, Proceedings of the 1997 International Conference on Neural Networks (ICNN), volume 1, pp. 81–87., Houston, Texas, 1997.

## Workshop Papers

Daniel A. Jiménez, *The Subconscious Mind of a Branch Predictor*, Wild and Crazy Ideas VI (WACI-VI) (co-located with ASPLOS XII), Seattle, Washington, March 2008.

Chunling Hu, John McCabe, Daniel A. Jiménez and Ulrich Kremer, *Infrequent Basic Block-based Program Phase Classification and Power Behavior Characterization*, Proceedings of the 10th IEEE Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-2006), February, 2006.

Chunling Hu, John McCabe, Daniel A. Jiménez and Ulrich Kremer, *The Camino Compiler Infrastructure*, Proceedings of the 2005 Workshop on Binary Instrumentation and Applications (WBIA), September, 2005.

Gabriel H. Loh and Daniel A. Jiménez, *Reducing the Power and Complexity of Path-Based Neural Branch Prediction*, Proceedings of the 2005 Workshop on Complexity-Effective Design (WCED'05), June, 2005.

Chunling Hu, Daniel A. Jiménez and Ulrich Kremer, *Toward an Evaluation Infrastructure for Power and Energy Optimizations*, Proceedings of the First Workshop on High-Performance, Power-Aware Computing, April 2005.

Daniel A. Jiménez, *Idealized Piecewise Linear Branch Prediction*, The First JILP Championship Branch Prediction Competition (CBP-1) (co-located with MICRO-37), December 2004.

Ravi Batchu and Daniel A. Jiménez, *Exploiting Procedure Level Locality to Reduce Instruction Cache Misses*, Proceedings of the 8th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-8), Madrid, Spain, February 15, 2004.

Daniel A. Jiménez and Calvin Lin, *Branch Path Re-Aliasing*, Proceedings of the 4th Workshop on Feedback Directed and Dynamic Optimization (FDDO-4), Austin, TX, December 2001.

## Other Publications

Ravi Batchu and Daniel A. Jiménez, *Exploiting Procedure Level Locality to Reduce TLB Overhead*, DCS-TR-XXX, Department of Computer Science, Rutgers University, May 2004 (TR number pending).

Daniel A. Jiménez, *Composite Confidence Estimators for Enhanced Speculation Control*, DCS-TR-XXX, Department of Computer Science, Rutgers University, May 2004 (TR number pending).

Ravi Batchu and Daniel A. Jiménez, *Exploiting Procedure Level Locality to Reduce Instruction Cache Misses*, technical report DCS-TR-532, Department of Computer Science, Rutgers University, July, 2003.

Nitya Ranganathan, Ramadass Nagarajan, Daniel Jiménez, Doug Burger, Stephen W. Keckler, and Calvin Lin, *Combining Exit Prediction and Hyperblocks to Improve Front-End Bandwidth and Performance*, technical report TR-02-41, Department of Computer Sciences, The University of Texas at Austin, September 2002.

Samuel Z. Guyer, Daniel A. Jiménez, and Calvin Lin, *The C-Breeze Compiler Infrastructure*, technical report TR-01-43, Department of Computer Sciences, The University of Texas at Austin, 2001.

Daniel A. Jiménez, *Delay-Sensitive Branch Predictors for Future Technologies*, Doctoral dissertation, Department of Computer Sciences, The University of Texas at Austin, 2001.

Daniel A. Jiménez, Tom Darm, Bill Rogers and Nicolas Walsh, *A Method for Locating BK Anatomical Landmarks for a Laser Scanning Imager* (invited paper), Proceedings of the International Symposium on CAD/CAM Systems in Pedorthics, Prosthetics and Orthotics, Nürnberg, Germany, 1997.

Daniel A. Jiménez, *Methods for Satisfying Hard Boolean Formulas*, Master's thesis, Division of Mathematics, Computer Science, and Statistics, The University of Texas at San Antonio, May 1994.

Alex López-Ortiz, Daniel A. Jiménez, *Comp.Theory FAQ*, a frequently-asked questions (FAQ) list for the Usenet newsgroup **comp.theory**, at <http://db.uwaterloo.ca/~alopez-o/comp-faq/faq.html>

Daniel A. Jiménez, *Program a RAM Disk*, Rainbow: The Color Computer Monthly Magazine, January, 1989.

## Invited Talks

*Efficient Power Behavior Characterization*, High-Performance Computing Group Seminar, Department of Computer Architecture, Technical University of Catalonia (UPC), Barcelona, Spain, May 2007.

*Recent Advances in Branch Prediction*, TU Delft, May 2006, Ghent University, May 2006, Technical University of Barcelona, May 2006, University Complutense of Madrid, May 2007, University of Edinburgh, May 2007.

*Code Placement for Improving Dynamic Branch Prediction Accuracy*, Intel Microprocessor Research Laboratory, Barcelona, Spain, August 2005.

*Idealized Piecewise Linear Branch Prediction*, High-Performance Computing Group Seminar, Department of Computer Architecture, Technical University of Catalonia (UPC), Barcelona, Spain, February 2005.

*Perceptrons for Dummies*, The First JILP Championship Branch Prediction Competition (CBP-1) (co-located with MICRO-37), Portland, Oregon, December 2004.

*Dynamic Branch Prediction with Perceptrons*, at Research, Careers, and Computer Science: A Maryland Symposium, Department of Computer Science, The University of Maryland, College Park, Maryland, November 2001.

*Delay Sensitive Branch Predictors*, Dept. de Arquitectura de Computadores, Universidad Politécnica de Catalunya, Barcelona, Spain, September 2001.

*A Method for Locating BK Anatomical Landmarks for a Laser Scanning Imager*, at the International Symposium on CAD/CAM Systems in Pedorthics, Prosthetics and Orthotics, Nürnberg, Germany, 1997.

## Selected Presentations

*Piecewise Linear Branch Prediction*, The 32nd International Symposium on Computer Architecture (ISCA-32), Chicago, Illinois, June 2005.

*Code Placement for Improving Dynamic Branch Prediction Accuracy*, The ACM SIGPLAN 2005 Conference on Programming Language Design and Implementation (PLDI), Madison, Wisconsin, 2005.

*Idealized Piecewise Linear Branch Prediction*, The First JILP Championship Branch Prediction Competition (CBP-1) (co-located with MICRO-37), Portland, Oregon, December 2004.

*Exploiting Procedure Level Locality to Reduce Instruction Cache Misses*, at the 8th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT-8), Madrid, Spain, February 15, 2004.

*Fast Path-Based Neural Branch Prediction*, at the 36th International Symposium on Microarchitecture (MICRO-36), San Diego, California, December 2003.

*Reconsidering Complex Branch Predictors*, at the 9th International Symposium on High Performance Computer Architecture (HPCA-9), Anaheim, California, February 2003.

*Neural Methods for Dynamic Branch Prediction*, at the Annual Current DCS Research Seminar, Rutgers University, November, 2002.

*Branch Path Re-Aliasing*, at the 4th Workshop on Feedback Directed and Dynamic Optimization (FDDO-4) (co-located with MICRO-34), December, 2001

*Boolean Formula-based Branch Prediction for Future Technologies*, at the International Conference on Parallel Architectures and Compilation Technologies (PACT), Barcelona, Spain, September 2001.

*Dynamic Branch Prediction with Perceptrons*, at the 7th International Symposium on High Performance Computer Architecture (HPCA-7), Monterrey, Mexico, January, 2001.

*The Impact of Delay on the Design of Branch Predictors*, at the 33rd Annual International Symposium on Microarchitecture (MICRO-33), Monterey, California, December, 2000.

*Locating Anatomical Landmarks for Prosthetics Design using Ensemble Neural Networks*, at the International Conference on Neural Networks (ICNN), Houston, Texas, 1997.

## **Departmental Service**

Member, UT San Antonio Department of Computer Science Curriculum Committee, 2008

Member, UT San Antonio Department of Computer Science Departmental Faculty Review Advisory Committee, 2007-present

Member, Rutgers DCS Graduate Admissions Committee, 2003

Member, Rutgers DCS Graduate Admissions Committee, 2004

Member, Rutgers DCS Graduate Program Committee, 2005-2006

## **Grants**

NSF CCF-0829760, "Systems Research Mentoring Workshop," \$25,000 effective May 1, 2008 (co-PI).

NSF CNS-0751138, "CRI: IAD Resources for Branch Prediction Research," \$233,730, effective June 1, 2008 (PI).

NSF CCF-0545898, "CAREER: Branch Prediction," \$400,000, effective as of April, 2006 (PI).

Ministerio de Educación y Ciencia (Spanish Ministry of Education and Science) SB2003-0357, "Ayudas para movilidad de Profesores de Universidad e Investigadores españoles y extranjeros" (Mobility assistance for Spanish and foreign university professors and researchers), with Mateo Valero, approved as of August 2004.

NSF CSA-0311091, "Improving Microarchitectural Performance with Neural Predictors," \$224,916, July 2003 through June 2006 (PI).

Rutgers Information Sciences and Technology Council, "An Evaluation Infrastructure for Power and Energy Optimizations," with Ulrich Kremer, \$30,294, May 2003 through April 2004 (co-PI).

## **Teaching (at Rutgers)**

CS673 - Readings in Instruction-Level Parallelism, Spring 2003.

CS507 - Advanced Computer Architecture, Fall 2006.

CS505 - Computer Structures, Fall 2002, Fall 2003, Fall 2004, Spring 2006.

CS211 - Computer Architecture, Spring 2004, Fall 2005, Spring 2006.

CS500 - Light Seminar: Machine Learning in Computer Architecture and Compilers, Fall 2004.

## **Teaching (at UTSA)**

CS1073 - Introductory Computer Programming for Scientific Applications, Fall 1996.

CS1713 - Introduction to Computer Science, Spring 1997, Summer 1997, Fall 1997.

CS1723 - Data Structures, Spring 1994, Summer 1998.  
CS2073 - Computer Programming with Engineering Applications, Fall 1992, Spring 1993, Fall 1997, Spring 2007.  
CS2083 - Microcomputer Applications, Fall 1993, Spring 1994.  
CS2733 - Computer Organization II, Fall 2007.  
CS2743 - Data Structures II, Spring 1993.  
CS3343 - Analysis of Algorithms, Spring 1998, Summer 2007.  
CS3843 - Computer Organization, Fall 2008.  
CS5513 - Computer Architecture, Fall 2007.

### **Doctoral Committees**

Chunling Hu, "An Infrastructure for Program Power Behavior Characterization and Optimization Evaluation," supervising professor, Summer 2007.  
Ravi V. Batchu, "Temporal Locality at Procedure Level – Its Study and Exploitation," supervising professor, Fall 2003  
Veerle Desmet, "On the Systematic Design of Cost-Effective Branch prediction," Ghent University, Belgium, (supervising professor Koen De Bosschere) Spring 2006.

### **Qualifying Examination/Proposal Committees**

Eduardo Pinheiro, "Power and Energy Conservation for Clusters," Fall 2002.  
Xiaoyan Li, "Using Adaptive Range Control to Optimize 1-hop Broadcast Coverage in Dense Wireless Sensor Networks," Summer 2003.  
Chen Fu, "Testing of Java Web Services for Robustness," Spring 2004.  
Chunling Hu, "Title: Toward an Evaluation Infrastructure for Power and Energy Optimizations," co-supervising professor, Fall 2004.  
Lei Wang, "Optimally Balanced Forward Degree Sequence," Spring 2006.  
Nitya Ranganathan, "Control Flow Prediction for Distributed Architectures," Spring 2007 (thesis proposal at UT Austin).

### **Master's Essays**

Timothy Munar, "Hardware Implementation of Data Prefetching," Spring 2003.  
Peng Zhou, "Performance from Hardware: Different Choices of Microarchitectural CPU Parameters," Spring 2003.  
Abhishek Mehrotra, "Optimizing on-chip memory allocation to maximize performance," Spring 2004.  
Charles Ganansia, "Fast Binary Addition," Spring 2004.  
Kris Rutkowski, "Branch Prediction for Sorting Algorithms," Spring 2004.

### **Professional Activities**

Co-Chair, CRA-W/CDC Mentoring Workshop for Systems Research, The University of Delaware, June 2008.  
Reviewer, 22nd ACM International Conference on Supercomputing (ICS-2008).

Reviewer, 22nd ACM International Conference on Supercomputing (ICS-2008).

Reviewer, ACM SIGPLAN 2008 Conference on Programming Language Design and Implementation (PLDI).

Reviewer, 2008 International Symposium on Code Generation and Optimization (CGO).

Reviewer, 13th International Symposium on High-Performance Computer Architecture (HPCA-2007).

Guest Editor, Journal of Instruction-Level Parallelism (JILP), 2007.

Program Committee Member, 21st ACM International Conference on Supercomputing (ICS-2007).

Panelist, NSF [program name redacted], 2007.

Co-Chair, CRA-W/CDC Programming Languages Summer School, The University of Texas at Austin, May 2007.

Chair, 2nd Championship Branch Prediction Workshop (CBP-2006).

Program Committee Member, 20th ACM International Conference on Supercomputing (ICS-2006).

Program Committee Member, 33rd International Symposium on Computer Architecture (ISCA-2006).

Publications Chair, 37th International Symposium on Microarchitecture (MICRO-2004).

Program Committee Member, 38th International Symposium on Microarchitecture (MICRO-2005).

Program Committee Member, 14th International Symposium on Parallel Architectures and Compilation Techniques (PACT-2005).

Program Committee Member, 13th International Symposium on Parallel Architectures and Compilation Techniques (PACT-2004).

Program Committee Member, 10th International Conference on High Performance Computing (HiPC-2003).

Reviewer, 39th International Symposium on Microarchitecture (MICRO-2006).

Reviewer, Journal of Systems Architecture (JSA), 2006.

Reviewer, 12th International Symposium on High-Performance Computer Architecture (HPCA-2006).

Reviewer, Journal of Machine Learning Research, 2005.

Reviewer, 2005 International Conference on High Performance Embedded Architectures and Compilers (HiPEAC 2005).

Reviewer, ACM Transactions on Architecture and Code Optimization (ACM TACO).

Reviewer, 12th International Conference on High Performance Computing (HiPC-2005).

Reviewer, 32th International Symposium on Computer Architecture (ISCA-2005).

Reviewer, 2005 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS).

Reviewer, 11th International Symposium on High-Performance Computer Architecture (HPCA-2005).

Reviewer, ACM SIGPLAN 2004 Conference on Programming Language Design and Implementation (PLDI).

Reviewer, 31th International Symposium on Computer Architecture (ISCA-2004).

Reviewer, Journal of Instruction-Level Parallelism (JILP), 2004.

Reviewer, 2004 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS).

Reviewer, 12th International Symposium on Parallel Architectures and Compilation Techniques (PACT-2003).

Reviewer, IEEE Transactions on Computers, 2003, 2008.

Reviewer, 36th International Symposium on Microarchitecture (MICRO-2003).

Reviewer, 30th International Symposium on Computer Architecture (ISCA-2003).

Reviewer, 2003 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS).

Reviewer, Journal of Instruction-Level Parallelism (JILP), 2003.

Reviewer, 29th International Symposium on Computer Architecture (ISCA-2002).

Reviewer, 10th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS).

Reviewer, 34th International Symposium on Microarchitecture (MICRO-2001).

Reviewer, 10th International Symposium on Parallel Architectures and Compilation Techniques (PACT-2001).

Reviewer, 2001 European Conference on Parallel Computing (EUROPAR).

Reviewer, IEE Proceedings on Computers and Digital Techniques

Reviewer, Journal of Parallel and Distributed Computing (JPDC).

Reviewer, Archives of Physical Medicine and Rehabilitation.

Member of the Association for Computing Machinery, 1999 - present

Member of IEEE and IEEE Computer Society, 2002 - present

Assistant Instructor, University of Texas WTF Taekwondo Club, 2000 - 2002

## **Awards and Honors**

2001–2002	Intel Foundation Graduate Fellowship, The University of Texas at Austin
1999	TA Service Commendation, Department of Computer Sciences, The University of Texas at Austin
1990–1992	Research Careers for Minority Scholars Scholarship, The University of Texas at San Antonio
August 15, 2008	